REMARKS

Claims 1-9 are canceled, and Claims 12-13 are added. Thus, Claims 10-13 are currently pending in the present application, of which Claims 10-11 have been amended.

Support for the claim amendments can be found on page 6, line 19 - page 7, line 15 of the specification.

Claims 2-3, 5 and 8 have been canceled. Thus, the claim objections are deemed moot.

Rejection under 35 U.S.C. § 112

Claim 11 was rejected under 35 U.S.C. § 112, second paragraph, for not particularly pointing out and distinctly claiming the subject matter that Applicants regard as the invention. Applicant respectfully traverses such rejection insofar as it might apply to the claims as amended herein.

The dependency of Claim 11 has been amended from Claim 1 to Claim 10, as suggested by the Examiner. Thus, the § 112 rejection is believed to be overcome.

Rejection under 35 U.S.C. § 102

Claims 1-3 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Sarnikowski et al.* (US 6,453,406).

Claims 1-3 have been canceled. Thus, the § 102 rejection is deemed moot.

Rejection under 35 U.S.C. § 103

Claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Drewlo et al.* (US 4,748,617) in view of *Szymanski et al.* (US 6,016,211). Applicant respectfully traverses such rejection insofar as it might apply to the claims as amended herein.

Amended Claim 10 now recites "a decoder array ... for converting said serial data stream to a corresponding set of parallel data" and "an electrical interface ... receives parallel data from said one receiver buffer and sends said parallel data to said electrical device, wherein said electrical interface directs parallel data received from said electrical device to one of said send buffers."

On page 6 of the Office Action, the Examiner asserts that the claimed decoder array and the claimed electrical interface are disclosed by *Drewlo* as logical transmitter **96** and high-speed serial data lines, respectively, in Figure **2**. However, logical transmitter **96** cannot convert "serial data stream to a corresponding set of parallel data," as claimed. Also, since high-speed serial data lines, such as **80**, **82**, **84**, **86**, **126**, **128**, **130** and **132**, are serial data lines, they are incapable of receiving "parallel data from said one receiver buffer" and directing "parallel data received from said electrical device to one of said send buffers," as claimed.

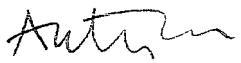
Because the claimed invention recites novel features that are not found in the cited references, whether considered separately or in combination, the § 103 rejection is believed to be overcome.

CONCLUSION

Claims 10-13 are currently pending in the present application. For the reasons stated above, Applicant believes that independent Claim 10 along with its dependent claims are in condition for allowance. The remaining prior art cited by the Examiner but not relied upon has been reviewed and is not believed to show or suggest the claimed invention.

No fee or extension of time is believed to be necessary; however, in the event that any addition fee or extension of time is required for the prosecution of the present application, please charge it against BAE Deposit Account No. **19-0130**.

Respectfully submitted,



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